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Docket No. YO999-598

REMARKS

Entry of this Amendment if proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 1-39 are presently pending in this application. Claims 1-13, 15-34, and 36-39 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 22-39 were rejected under 35 U.S.C. §101 as directed to non-statutory subject matter due to the claims appearing to be directed to a system and also to a method. This has been corrected by indicating the claims to be directed to a system. Thus, this rejection is overcome.

Claims 1-39 were rejected under 35 U.S.C. §112, first and second paragraphs due to expressions in the claims, such as "less-to-more granular," "simultaneously," "optimizes," and "concurrently" which are used throughout the application, although perhaps not commonly used in the industry. The claims have been amended to use more commonly-used expressions. Accordingly, this rejection is overcome.

Claims 1-15 and 22-37 were rejected under 35 U.S.C. §102(e) as being anticipated by Shenoy (U.S. Patent No. 6,378,114). This rejection is respectfully traversed.

In exemplary embodiments, the claimed invention is directed to a method and a

system for modifying a plurality of domains of a circuit. The domains include at least one of a Boolean domain, an electrical domain, and a physical domain. In a preferred embodiment of the method, exemplified by claim 1, a set of steps of placement and netlist modification transforms is applied in a flexible sequence. Each transform includes a plurality of steps. The impact of the sequence of the set of steps of the modification transforms is evaluated. Sequences that, upon evaluation, do not improve the design space are rejected. This is repeated to create a design process flow to meet design performance targets.

A preferred embodiment of the system, exemplified by claim 22, accomplishes this method.

Another preferred embodiment, exemplified by claim 16, is directed to a method of applying transformations during placement synthesis interaction, and includes creating and updating bins, and applying a plurality of transforms on a bin-based database updated by both placement and synthesis, each transform including a plurality of steps, updating the bin-based timing, invoking a synthesis-placement scenario, selecting synthesis and placement transforms, invoking steps of selected transforms within the scenario, and applying transforms that change the design space.

In other embodiments, the claimed invention includes programmable storage media tangibly embodying a program of machine-readable instructions to carry out the claimed method.

Shenoy discloses a method for the physical placement of an integrated circuit adaptive to netlist changes. Shenoy's method is exemplified by his Figures 1 and 3. Shenoy's method initially performs synthesis (step 304) and mapping (step 305). Then the method iterates

through a given sequence of cell separation, synthesis or netlist tweaking, and partitioning.

In Shenoy's method, synthesis or netlist tweaking utilizes a single step to combine numerous actions. By way of example, logic synthesis is done in one step. The whole synthesis process is interleaved with a physical design step – that of cell separation and partitioning. Shenoy's steps 103, 105, and 106 are specific physical domain optimizations and are applied in a specific sequence with step 104.

In contrast, in the claimed invention, each transform includes a plurality of steps which are applied in a flexible sequence. Individual steps of synthesis and physical design are interleaved throughout the design process. The impact of the sequence of the set of steps is evaluated, and sequences that do not improve the design space are rejected. Thus, the claimed invention provides greater flexibility, and so more assuredly results in creating of a design process flow to meet design performance targets. These aspects of the invention are set forth in the claims.

In view of the foregoing, Applicant submits that claims 1-39, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper,

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including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

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